Ahsanullah University of Science and Technology

Department of Electrical and Electronic Engineering

LABORATORY MANUAL

FOR

ELECTRICAL AND ELECTRONIC SESSIONAL COURSES

Student Name :

Student ID :

Course No. : EEE 2286

Course Title : Analog and Digital Electronics Sessional

For the students of

Department of Mechanical Engineering

2nd Year, 2nd Semester

Table of Contents

Experiment No: 01

Name of the Experiment : I-V Characteristics of diode.

Objective :

Study the I-V characteristic of diode.

Theory :

A diode is a bi-polar device that behaves as the short circuit when it is in forward bias and as an open circuit when it is in reverse bias condition.

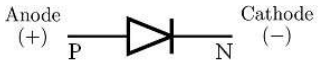


Figure 1.1 : Schematic Diagram of Diode.

Figure 1.2 : P - N Junction Diode .

There are two types of biasing condition for a diode :

1. When the diode is connected across a voltage source with positive polarity of source connected to p side of diode and negative polarity to n side, then the diode is in forward bias condition.

2. When the diode is connected across a voltage source with positive polarity of source connected to n side of diode and negative polarity to p side, then the diode is in reverse bias condition.

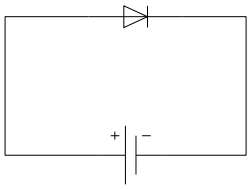


Figure 1.3 : Forward Bias connection.

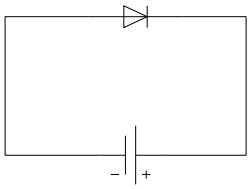


Figure 1.4 : Reverse Bias connection.

If the input voltage is varied and the current through the diode corresponds to each voltage are taken then the plot of diode current (I_d) vs diode voltage (V_D) will be follows :

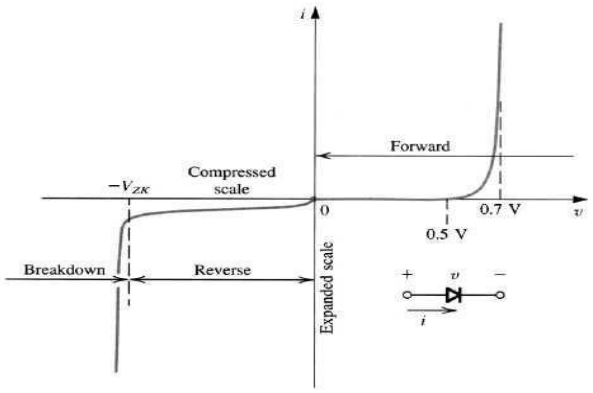


Figure 1.5 : I - V Characteristics of Diode.

At the reverse bias condition the amount of current flows through the diode is very small (at microampere range). But if the voltage continuously increases in reverse direction, at a certain value the diode will break down and huge amount of current will flow in reverse direction. This is called breakdown of diode. In laboratory the breakdown will not tested because it will damages the diode permanently.

From the characteristics curve it can be seen that, a particular forward bias voltage (V_T) is required to reach the region of upward swing. This voltage, V_T is called the cut-in voltage or threshold voltage of diode. For Si diode the typical value of threshold voltage is 0.7 volt and for Ge diode is 0.3 volt.

Equipments And Components :

Serial no.	Component Details	Specification	Quantity
1.	p-n junction diode	1N4007	1 piece
2.	Resistor	1KΩ	1 piece
3.	DC power supply		1 unit
4.	Signal generator		1 unit
5.	Trainer Board		1 unit
6.	Oscilloscope		1 unit
7.	Digital Multimeter		1 unit
8.	Chords and wire		as required

Experimental Setup :

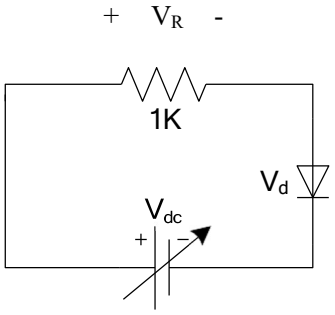


Figure 1.6 : Circuit Diagram for Obtaining Diode Obtaining Diode Forward Characteristics.

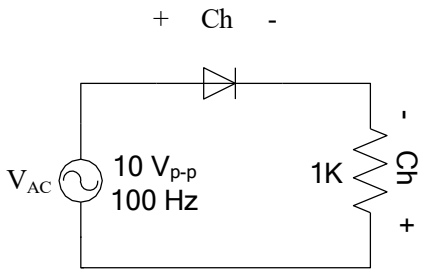


Figure 1.7 : Circuit Diagram for Characteristics From Oscilloscope.

Procedure :

1. Measure the resistance accurately using multimeter.
2. Construct the circuit as shown in figure - 1.6.
3. Vary input voltage V_{dc}. Measure V_{dc}, V_d, V_R for the given values of V_d and record data on data table. Obtain maximum value of V_d without increasing V_{dc} beyond 25 volt.
4. Calculate the values of I_d using the formula, $I_d = V_R / R$.
5. Construct the circuit as shown in figure - 1.7.
6. Ste the oscilloscope in X-Y mode. Identify zero record on oscilloscope display. Make proper connection and observe the output.
7. Repeat the step 5 and 6 by increasing the input supply frequency 5 KHz.

Data Table :

V_{dc} (volt)	V_d (volt)	V_R (volt)	$I_d = V_R / R$ (mA)

Report :

1. Draw the I - V characteristics curve of diode from the reading obtain in this experiment.
2. Calculate static resistance for I_d = 5 mA and I_d = 10 mA.
3. Determine the Q- point for the circuit in figure – 1.6, when V_{dc} = 3 volt.

Experiment No: 02

Name of the Experiment : The output characteristics of CE (common emitter) configuration of BJT.

Objective:

Study of the output characteristics of CE (common emitter) configuration of BJT.

Theory :

Unlike the diode, which has two doped region, a transistor has three doped region. They are as follows –

a) Emitter,
b) Base and
c) Collector.

These three doped regions form two junctions: One between the emitter and base and other between the collector and the base. Because of these it can be thought as combination of two diodes, the emitter and the base form one diode and the collector and base form another diode. The emitter is heavily doped. Its job is to emit or inject free majority carrier (electron for NPN and hole for PNP) into the base. The base is lightly doped and very thin. It passes the most of the emitter-injected electron (for NPN) into the collector. The doping level of the collector is between emitter and base. Figure 5.1 shows the biased NPN transistor.

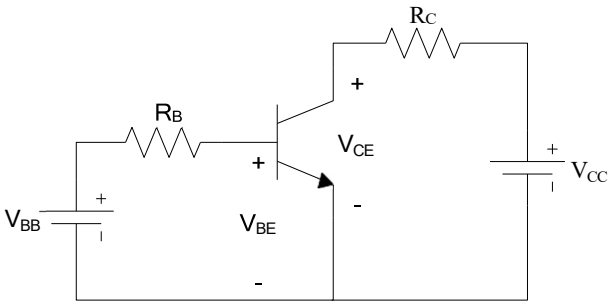


Figure 2.1 : Biasing of an NPN transistor.

If the V_{BB} is greater than the barrier potential, emitter electron will enter base region. The free electron can flow either into the base or into the collector. As base lightly doped and thin, most of the free electron will enter into the collector.
There are three different current in a transistor. They are emitter current (I_E), collector current (I_C) and the base current (I_B) are shows in figure 5.2.

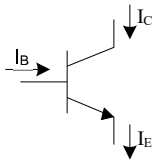


Figure 2.2 : Different current in transistor.

Here, $I_E = I_C + I_B$, and the current gain $\beta = \frac{I_C}{I_B}$

Characteristics Curve : The characteristics of a transistor is measured by two characteristics curve. They are as follows –

a) Input characteristics curve.
b) Output characteristics curve.

Input Characteristics Curve : Input characteristics is defined as the set of curves between input current (I_B) vs. input voltage (V_{BE}) for the constant output voltage (V_{CE}). It is the same curve that is found for a forward biased diode.

Output Characteristics Curve : Output characteristics is defined by the set of curves between output current (I_C) vs. output voltage (V_{CE}) for the constant input current (I_B). The curve has the following features –

- It has three regions namely Saturation, Active and Cutoff region.
- The rising part of the curve, where V_{CE} is between 0 and approximately 1 volt is called saturation region. In this region the collector diode is not reversed biased.
- When the collector diode of the transistor becomes reverse biased, the graph becomes horizontal. In this region the collector remains almost constant. This region is known as the active region. In applications where the transistor amplifies weak radio and TV signal, it will always be operation in the active region.
- When the base current is zero, but there is some collector current. This region of the transistor curve is known as the cutoff region. The small collector current is called collector cutoff current.
- For different value of base current (I_B) an individual curve can be obtained.

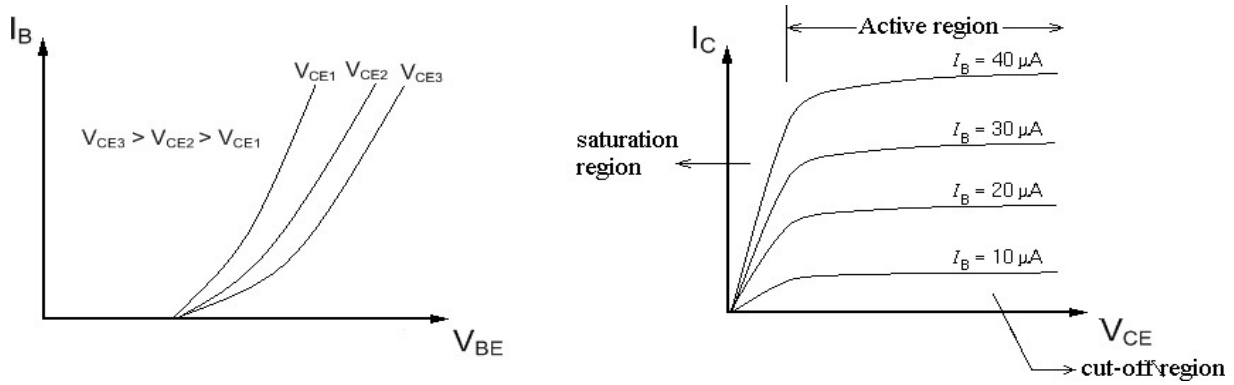


Figure 2.3 : (a) Input Characteristic, (b) Output Characteristic of NPN transistor.

Equipments And Components:

Serial no.	Component Details	Specification	Quantity
1.	Transistor	C828	1 piece
2.	Resistor	470Ω, 2.2KΩ, 3.3KΩ, 4.7KΩ, 10KΩ, 470KΩ	1 piece each
3.	POT	100KΩ	1 unit
4.	Trainer Board		1 unit
5.	DC Power Supply		1 unit
6.	Digital Multimeter		1 unit
7.	Chords and wire		as required

Experimental Setup:

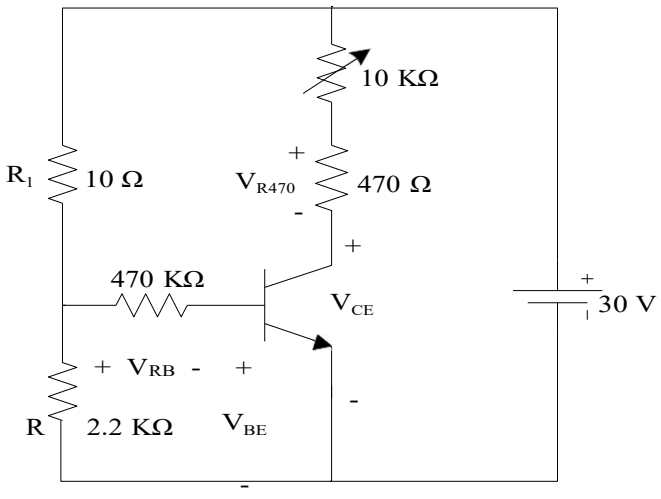


Figure 2.4: Experimental Circuit.

Procedure:

1. Connect the circuit as shown in the figure 5.4. Use 2.2 KΩ as R.
2. Measure V_{RB} and calculate I_S using $I_E = V_{RB} / R_B$. (We will assume that I_B to be constant for a particular setup at input.)
3. Measure the voltages of V_{CE} and V_{R470}. And calculate I_C using $I_C = V_{R470} / R_{470}$.

4. Take at least 10 reading by varying the POT.
5. Repeat step 1 to 4 with resistance R as 3.3 KΩ and 4.7 KΩ.

Table 5.1 : Data for I - V characteristics of transistor.

R (KΩ)	$I_B = V_{RB} / R_B$ (μA)	V_{CE} (volts)	V_{R470} (volts)	$I_C = V_{R470} / R_{470}$ (mA)
2.2				
3.3				
4.7				

Report:

1. Plot the graph of I_C vs. V_{CE} with necessary details. Show the different regions of operation.
2. Plot a hypothetical output characteristic using PNP transistor.
3. Find β for the three different condition.

Experiment No: 03

Name of the Experiment: The BJT Biasing Circuits.

Objective:

Study of the BJT Biasing Circuits.

Theory:

Biasing a BJT circuit means to provide appropriate direct potentials and currents, using external sources, to establish an operating point or Q-point in the active region. Once the Q-point is established, the time varying excursions of input signal should cause an output signal of same waveform. If the output signal is not a faithful reproduction of the input signal, for example, if it is clipped on one side, the operating point is unsatisfactory and should be relocated on the collector characteristics. Therefore, the main objective of biasing a BJT circuit is to choose the proper Q-point for faithful reproduction of the input signal. There are different types of biasing circuit. However, in the laboratory, we will study only the fixed bias and self bias circuit. In the fixed bias circuit, shown if figure 6.1, the base current I_B is determined by the base resistance R_B and it remains constant. The main drawback of this circuit is the instability of Q-point with the variation of β of the transistor. In the laboratory, we will test the stability using two transistors with different β. In the self bias circuit shown if figure 6.2, this problem is overcome by using the self biasing resistor R_E to the emitter terminal.

Equipments And Components :

Serial no.	Component Details	Specification	Quantity
1.	NPN Transistor	C828, BD135	1 piece each
2.	Resistor	470Ω, 560Ω, 220KΩ	1 piece each
3.	POT	10KΩ	1 unit
4.	Trainer Board		1 unit
5.	DC Power Supply		1 unit
6.	Digital Multimeter		1 unit
7.	Chords and wire		as required

Experimental Setup:

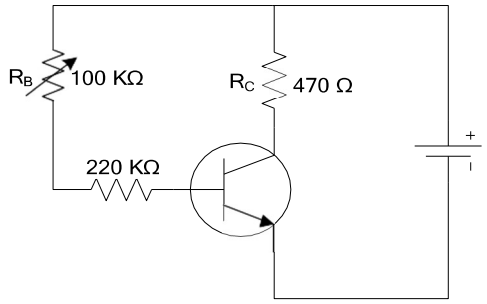


Figure 3.1: Experimental Circuit 1.

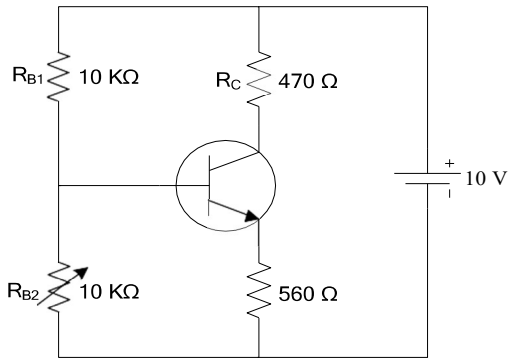


Figure 3.2: Experimental Circuit 2.

Procedure :

1. Arrange the circuit shown in figure - 6.1 by C828. Record R_C and set R_B to maximum value.
2. Decrease POT R_B gradually so that $V_{CE} = V_{CC} / 2$.
3. Measure voltage across R_C and V_{CE}.
4. Record the Q-point (V_{CE}, I_C).
5. Replace the C828 transistor by BD135 and repeat step 3 and 4.
6. Arrange the circuit shown in figure - 6.2 by C828. Record R_C and set R_B to minimum value.
7. Increase POT R_{B2} gradually so that $V_{CE} = V_{CC} / 2$.
8. Measure voltage across R_C and V_{CE}.
9. Record the Q-point (V_{CE}, I_C).
10. Replace the C828 transistor by BD135 and repeat step 8 and 9.

Data Sheet :

Table 6.1 : Data for Fixed Bias Circuit.

Transistor	R_C (Ω)	V_C (volt)	$I_C = V_C / R_C$ (Amp)	V_{CE} (volt)	Q-point
C828					
BD135					

Table 6.2 : Data for Self Bias Circuit.

Transistor	R_C (Ω)	V_C (volt)	$I_C = V_C / R_C$ (Amp)	V_{CE} (volt)	Q-point
C828					
BD135					

Report:

1. Which circuit shows better stability? Explain in the context of the results obtained in the laboratory.
2. Draw the DC load line for both the circuits and show the Q-point.

Experiment No: 04

Name of the experiment: Introduction to OPAMPs.

Introduction:

The operational amplifier (abbreviated as OPAMP) is a direct-coupled high-gain amplifier to which feedback is added to control its overall response characteristic. It has very high (ideally ∞) input impedance, very low (ideally 0) output impedance and large bandwidth and its characteristics do not drift with temperature. It offers all the advantages of monolithic integrated circuits: Small size, high reliability, reduced cost, temperature tracking and low offset voltage and current. For these reasons, it has gained wide acceptance as a versatile, predictable and economic system building block.

An OPAMP may be used to perform many mathematical operations. Some of these basic applications are studied in this experiment

Inverting adder adds up the signals at its inverting input terminal and produces the inverse of this summation at the output, provided, the value of the feedback resistance and the resistance in series with the input signals are chosen correctly.

Voltage follower produces almost the same output as is applied to its input. The input resistance of a voltage follower circuit is very high (several mega ohms). Therefore, it draws negligible current from a signal source. Thus it works as a voltage buffer that provides a means of isolating an input signal from a load.

An important feature that must be taken into account while designing circuits with OPAMPs is Slew rate. It is the time rate of change of the closed loop amplifier output voltage under large signal conditions. It tells how fast the output voltage of an OPAMP changes and limits the output frequency f_{max} for distorted output. The relation between f_{max} and slew rate is expressed as

$$f_{max} = \frac{slew\ rate}{2\pi \times V_0}$$

where, V_0 is the maximum distorted output voltage in volts, f_{max} is the maximum operable frequency in Hz and the slew rate is in volts per microsecond.

Equipments:

Serial no.	Component Details	Specification	Quantity
1.	OPAMP	741	1 piece
2.	Resistor	2.2 MΩ,100KΩ, 10kΩ	1 piece, 1piece, 4 pieces
3.	Oscilloscope		1 unit
4.	AC signal generator		1 unit
5.	DC Power Supply		3 units
6.	Digital Multimeter		1 unit
7.	Trainer Board		1 unit

Circuit Diagram:

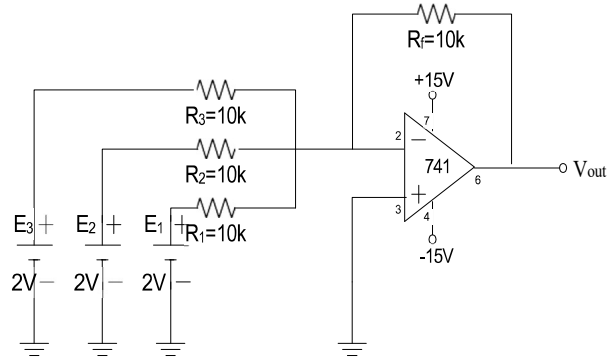


Fig 4.1

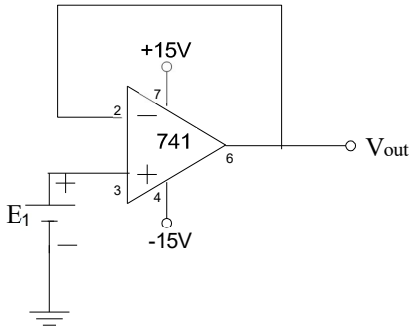


Fig 4.2

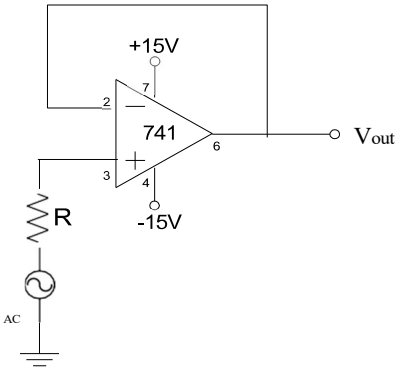


Fig 4.3

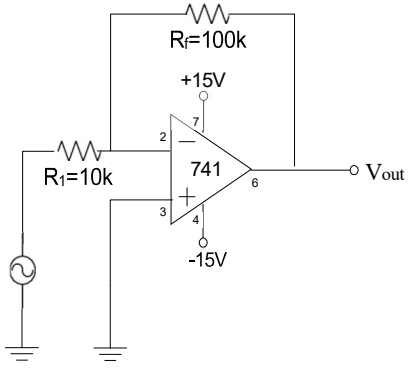


Fig 4.4

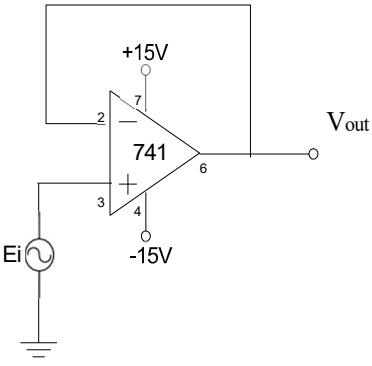


Fig 4.5

Procedure:

a) Study of inverting adder:

1) Connect the circuit of figure 1.1 and obtain values of V_0 for

- $E_1=E_2=E_3=2V$
- $E_1=3V$, $E_2=-3V$, $E_3=0V$
- $E_1=5V$, $E_2=-0V$, $E_3=2V$

2) Put $R_1=10K$, $R_2=20K$, $R_3=50K$, $R_f=100K$ and repeat step 1.

b) Study of the voltage follower:

1) Connect the circuit of figure 1.2 and measure V_0 for $E_1=4V$ and -4V.

2) To measure the input resistance of a voltage follower, change E_i to 5V rms at 100 Hz (sine wave) and connect R= 2.2MΩ in series with the source as shown in figure 1.3.

c) Measuring frequency response of small signal amplifier:

1) Connect the circuit of figure 1.4.

2) Adjust the input voltage E_2 to some convenient value, say 100mV (p-p)

3) Adjust the frequency to obtain undistorted maximum output. Measure the midband output voltage and calculate the voltage gain.

4) Keeping E_i constant, reduce the frequency until the output drops to 0.707 of its midband value and read the lower cut-off frequency, f_L. Next increase the frequency until the output again drops to 0.707 of its midband value and read upper cut-off frequency f_H.

5) Now connect E_1 to non-inverting terminal of figure 1.4 and following the above procedure to find f_L and f_H at this condition.

d) Slew Rate:

1) Connect the circuit of figure 1.5 and apply 10V (p-p) sinusoidal input E_i and increase the frequency until the output voltage, V_0 is distorted. Take readings for f_{max} and V_0.

2) Do the same with 1V (p-p) sinusoidal input.

Reports:

1) For inverting adder, do the experimental results support theory?
2) Calculate input resistance of voltage follower.
3) Calculate bandwidth for both cases in the experiment of frequency response measurement. Use Bandwidth B, f_H, f_L.
4) For OPAMP 741, slew rate is 0.5v/μS. Calculate maximum frequency for undistorted output with inputs 10V (p-p) and 1V (p-p). Compare them with the experimental results.

References:

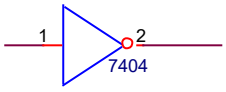
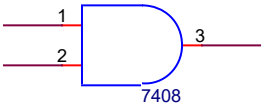
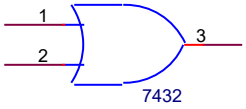
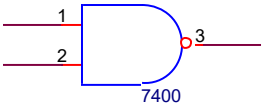
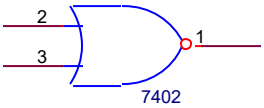
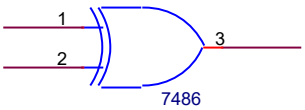
1) *Operational Amplifiers and Linear Integrated Circuits –Coughlin and Driscoll*
2) *Electronic Devices and Circuit Theory-Robert Boylestead*
3) *Integrated Electronics-Millman and Halkis*

Experiment: 05
Experiment name: Introduction to different digital ICs.

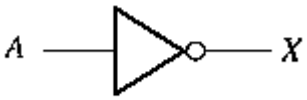
Introduction:

In this experiment you will be introduced to different digital ICs that will be used in this digital lab to perform different functions and also the function of each IC. You are asked to memorize the followings associated with each IC.

1. IC number
2. IC name
3. Total number of pins
4. V_{cc} pin number
5. Ground pin number

IC number	IC name	Schematic view
7404	NOT/INVERTER	
7408	AND	
7432	OR	
7400	NAND	
7402	NOR	
7486	XOR	

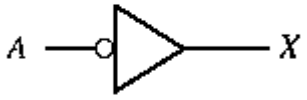
The INVERTER/NOT Gate



A	X
0	1
1	0

$X = \overline{A}$

Boolean expression



Distinctive shape symbols

Truth table

0 = LOW
1 = HIGH

The output of an inverter is always the complement (opposite) of the input.

The AND Gate

Distinctive shape symbol

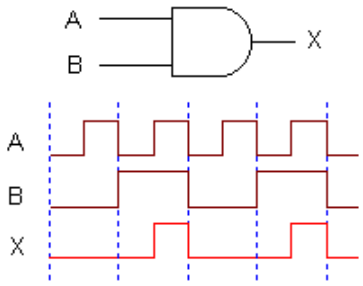
X = AB

Boolean expression

B	A	X
0	0	0
0	1	0
1	0	0
1	1	1

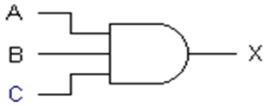
Truth table

0 = LOW
1 = HIGH



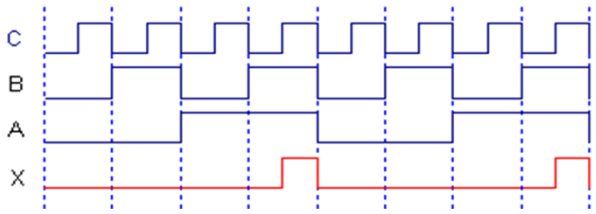
Pulsed Waveforms

The output of an AND gate is HIGH only when all inputs are HIGH.



X = ABC

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



3 Input AND Gate

The OR Gate

Distinctive shape symbol

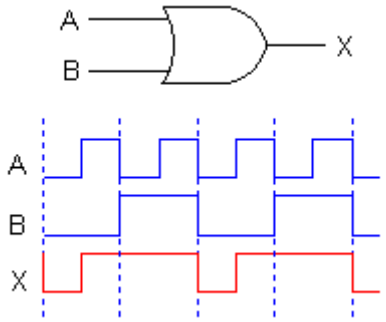
X = A + B

Boolean expression

B	A	X
0	0	0
0	1	1
1	0	1
1	1	1

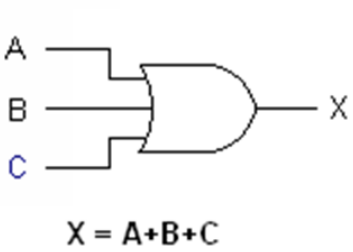
Truth table

0 = LOW
1 = HIGH



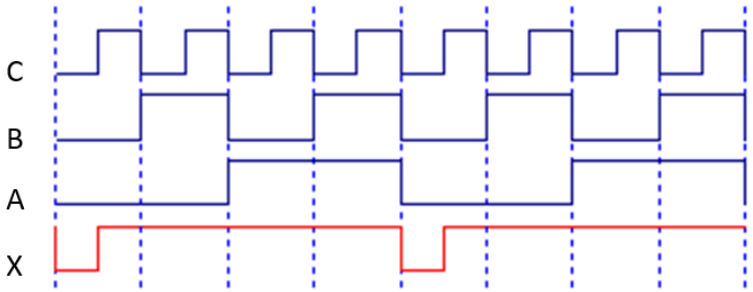
Pulsed Waveforms

The output of an OR gate is HIGH whenever one or more inputs are HIGH.



X = A+B+C

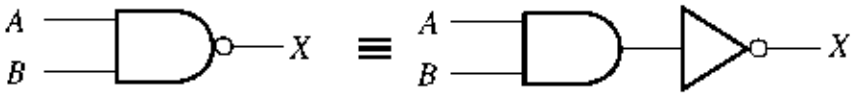
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



3 Input OR Gate

The NAND Gate

Distinctive shape symbol



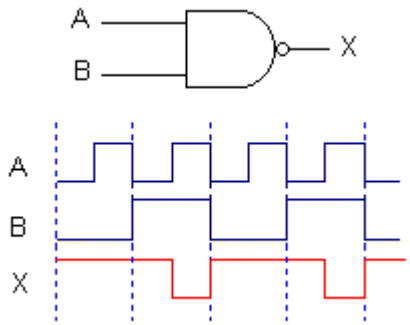
B	A	X
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

0 = LOW
1 = HIGH

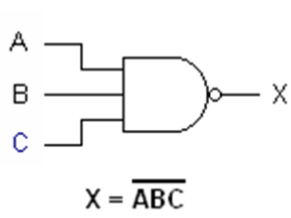
$X = \overline{AB}$

Boolean expression



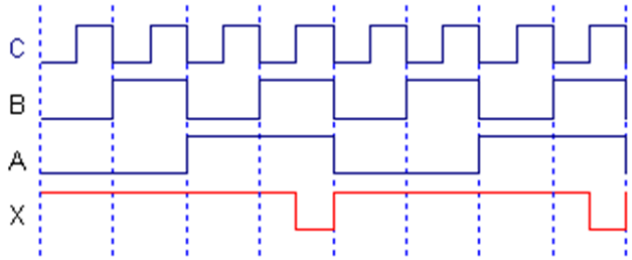
Pulsed Waveforms

The output of a NAND gate is HIGH whenever one or more inputs are LOW.



$X = \overline{ABC}$

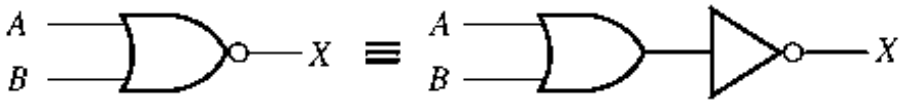
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



3 Input NAND Gate

The NOR Gate

Distinctive shape symbol



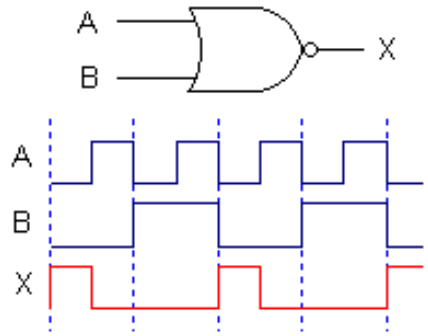
B	A	X
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

0 = LOW
1 = HIGH

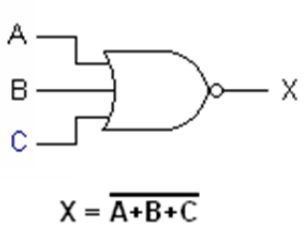
$X = \overline{A + B}$

Boolean expression



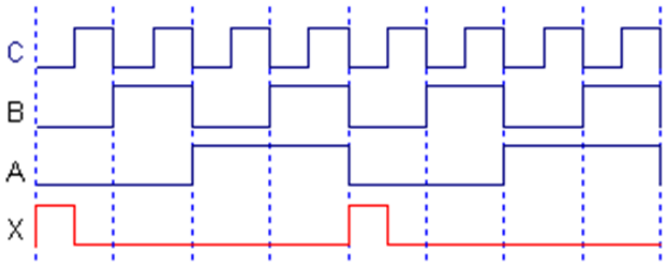
Pulsed Waveforms

The output of a NOR gate is LOW whenever one or more inputs are HIGH.



$X = \overline{A+B+C}$

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



3 Input NOR Gate

Exclusive-OR Gate

Distinctive shape symbol

B	A	X
0	0	0
0	1	1
1	0	1
1	1	0

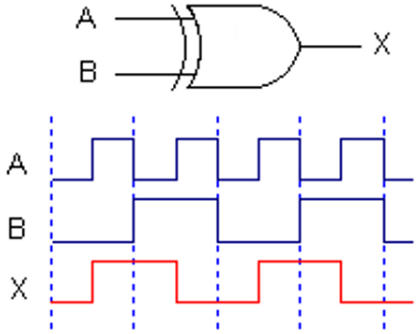
Truth table

0 = LOW
1 = HIGH

$X = A \oplus B$

Boolean expression

The output of an XOR gate is HIGH whenever the two inputs are different.



Pulsed Waveforms

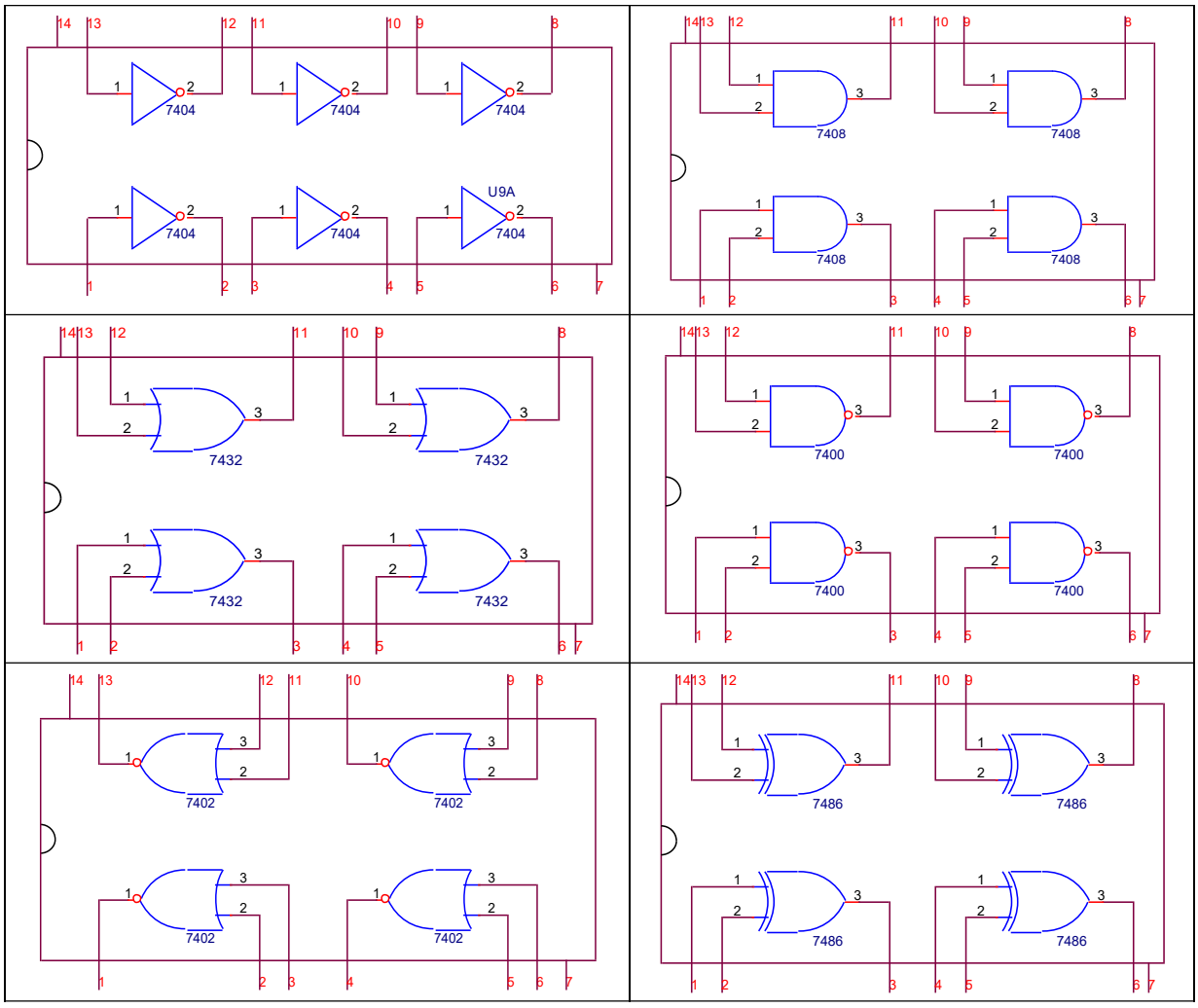
Equipment:

1. Trainer Board
2. IC 7400,7402,7404,7408,7432,7486
3. Microprocessor Data handbook

Procedure:

1. Take any of the following ICs. From microprocessor data handbook find the name of the IC, total number of pins that it has, V_{cc} pin and ground pin.

IC Number	**IC name**	**Total number of pin**	**V_{cc} pin no.**	**Ground pin no.**
7400	NAND	14	14	7
7402	NOR	14	14	7
7404	NOT	14	14	7
7408	AND	14	14	7
7432	OR	14	14	7
7486	XOR	14	14	7



2. Note the number of gates each IC has from the handbook.
3. Now fill up the following table:

Input A	**Input B**	**7400 NOT** $Y = \overline{A}$	**7432 OR** $Y = A + B$	**7402 NOR** $Y = \overline{A + B}$	**7486 XOR** $Y = A \oplus B$	**7408 AND** $Y = AB$	**7400 NAND** $Y = \overline{AB}$
0	0						
0	1						
1	0						
1	1						

4. Now verify the observed output with the desired output for different combination of inputs.
5. Repeat step 1 to 4 for different ICs.

Report:

1. How can you make a three input AND/OR/XOR gate with a two input AND/OR/XOR gate?
2. Is it possible to make a three input NAND/NOR gate with a two input NAND/NOR gate? Justify your answer.

Experiment: 06
Experiment name: Introduction to Combinational logic and K map minimization.

Introduction:

Logic design basically means the construction of appropriate function, presented in Boolean algebraic form, then edification of the logic diagram, and finally choosing of available ICs and implementing the IC connection so that the logic intended is achieved. The efficiency in simplifying the algebra leads to less complicated logic diagram, which in the end leads to easier IC selection and easier circuit implementation.

Caution:

1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs appropriate voltages to appropriate pins.

Equipment:

1. Trainer Board
2. IC 7400,7402,7404,7408,7432,7486
3. Microprocessor Data handbook

Job 1:

Implement of function $f = AB + BC' + CA$

$$= ABC + ABC' + ABC' + A'BC' + ABC + AB'C$$
$$= ABC + ABC' + A'BC' + AB'C$$
$$= m_7 + m_6 + m_2 + m_5$$
$$= \sum m(2,5,6,7)$$

Truth Table

Row no.	Input			Output
	A	B	C	*f*
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

K-Map

A \ BC	00	01	11	10
0	0	0	0	1
1	0	1	1	1

AC BC'

SOP: $F = AC + BC'$

POS: $F' = B'C' + A'C$

$\Rightarrow F = (B'C' + A'C)'$

$\Rightarrow F = (B + C)(A + C')$

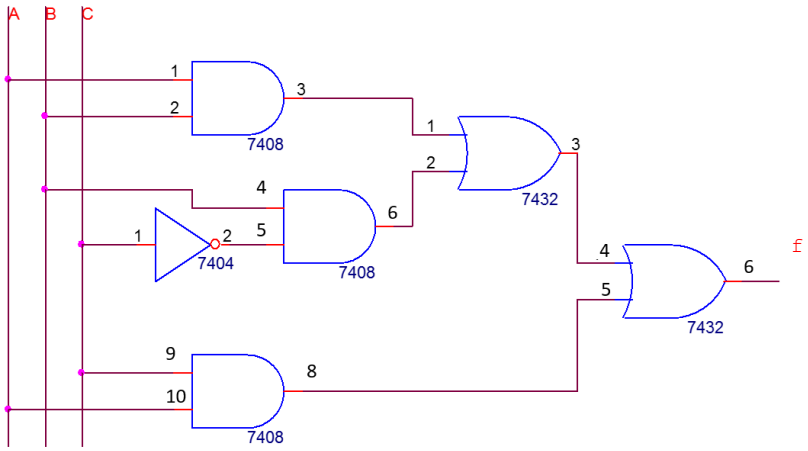


Figure 6.1: Logic Diagram of Job 1

Procedure:

1. Draw logic diagram to implement the function.
2. Select ICs from the equipment list.
3. Note the output logic for all combination of inputs.
4. Repeat step-1, 2 and 3 for SOP and POS function.

Job 2:

Implement of function $f = (AB + B)(C + A)(AC + B)$

Now,

$$
\begin{aligned}
f &= (AB + B)(C + A)(AC + B) \\
&= B(A + 1)(A + B)(A + C)(A + B)(B + C) \\
&= B(A + B)(A + C)(B + C) \\
&= (B + AA')(A + B)(A + C)(B + C) \\
&= (A + B)(A' + B)(A + B)(A + C)(B + C) \\
&= (A + B)(A' + B)(A + C)(B + C) \\
&= (A + B + CC')(A' + B + CC')(A + C + BB')(B + C + AA') \\
&= (A + B + C)(A + B + C')(A' + B + C)(A' + B + C')(A + B + C)(A + B' + C)(A + B + C)(A' + B + C) \\
&= (A + B + C)(A + B + C')(A' + B + C)(A' + B + C')(A + B' + C) \\
&= M_0 M_1 M_4 M_2 M_5 \\
&= \prod M\ (0,1,2,4,5)
\end{aligned}
$$

Distributive Law

$x + yz = (x + y)(x + z)$

Truth Table

Row no.	Input			Output
	A	B	C	*f*
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

K-MAP

A \ BC	00	01	11	10
0	0	0	**1**	0
1	0	0	**1**	**1**

BC **AB**

SOP: $F = AB + BC$

POS: $F' = B' + A'C'$

$\Rightarrow F = B(A + C)$

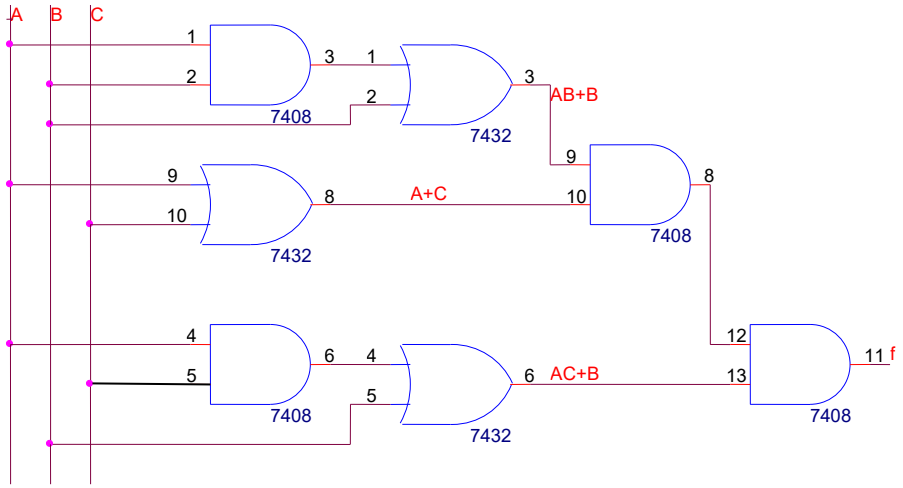


Figure 6.2: Logic Diagram of Job 2

Procedure:

1. Simplify the function in POS form and in SOP form by using Boolean algebra.
2. Draw logic diagram to implement the function.
3. Select ICs from the equipment list.
4. Note the output logic for all combination of inputs.

Experiment: 07

Experiment name: Construction of adders, subtractors , using basic logic gates.

Introduction:

Adders and sub tractors are the basic operational units of simple digital arithmetic operations. In this experiment, the students will construct the basic adder and sub tractor circuit with common logic gates and test their operability. Then in the last job, they will cascade adder ICs to get higher bit adders.

Binary Adder

Among the basic functions encountered are the various arithmetic operations. The most basic arithmetic operation, is the addition of two binary digits. This simple addition consists of four possible elementary operations, namely, 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, and 1 + 1 = 10. The first three operations produce a sum whose length is one digit, but when both augend and addend bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a *carry.* When the augend and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next higher-order pair of significant bits. A combinational circuit that performs the addition of two bits is called a *half-adder.* One that performs the addition of three bits (two significant bits and a previous carry) is *full-adder.*

Half Adder

From the basic understanding of a half-adder, we find that the circuit needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry. It is necessary to specify two output variables because the result may consist of two binary digits. We arbitrarily assign symbols *x* and *y* to the two inputs and S (for sum) and C (for carry) to the outputs.

Now that we have established the number and names of the input and output variables, we are ready to formulate a truth table to identify exactly the function of the half-adder. This truth table is

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The carry output is 0 unless both inputs are 1. The S output represents the least significant bit of the sum.

The simplified Boolean functions for the two outputs can be obtained directly from the truth table. The simplified sum of products expressions are

$$S = x'y + xy' = x \oplus y$$

$$C = xy$$

The logic diagram for this implementation is shown below

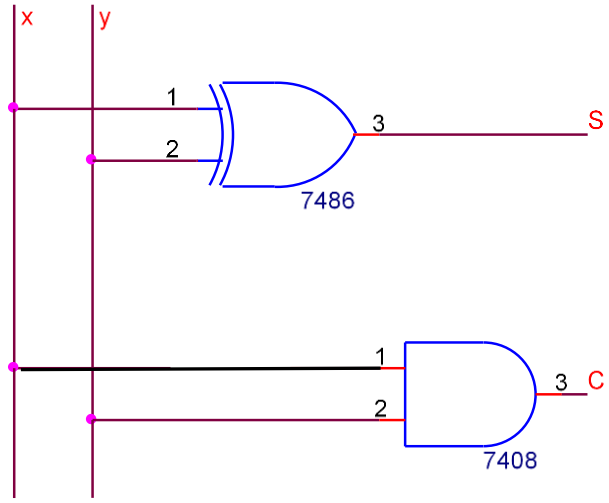


Fig 7.1. Half-adder

Full Adder

A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by *x* and *y,* represent the two significant bits to be added. The third input, z, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols S for sum and C for carry. The binary variable S gives the value of the least significant bit of the sum. The binary variable Cr gives the output carry. The truth table of the full-adder is

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The eight rows under the input variables designate all possible combinations of 1's and 0's that these variables may have. The 1's and 0's for the output variables are determined from the arithmetic sum of the input bits. When all input bits are 0's, the output is 0. The S output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1. The C output has a carry of 1 if two or three inputs are equal to 1. Physically, the binary signals of the input wires are considered binary digits added arithmetically to form a two-digit sum at the output wires. On the other hand, the same binary values are considered variables of Boolean functions when expressed in the truth table or when the circuit is implemented with logic gates. It is important to realize that two different interpretations are given to the values of the bits encountered in this circuit. The input-output logical relationship of the full-adder circuit may be expressed in two

Boolean functions, one for each output variable. This implementation uses the following Boolean expressions:

$$S = x'y'z + x'yz' + xy'z' + xyz = z'(x'y + xy') + z(x'y' + xy) = z'(x \oplus y) + z(x \oplus y)' = x \oplus y \oplus z$$
$$C = x'yz + xy'z + xyz' + xyz = x(y'z + yz') + yz(x + x') = x(y \oplus z) + yz$$

The logic diagram for the full-adder implemented in sum of products is shown in Fig. 2.2

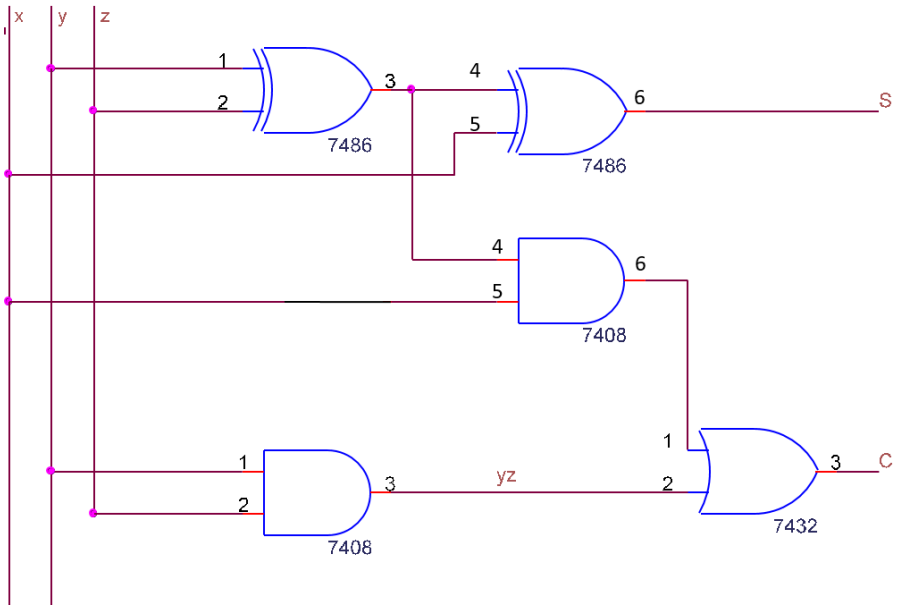


Fig 7.2. Full-adder

Half Subtractor

A half-subtractor is a combinational circuit that subtracts two bits and produces their difference. It also has an output to specify if a 1 has been borrowed. Designate the minuend bit by *X* and the subtrahend bit by *y.* To perform *x* - *y,* we have to check the relative magnitudes of *x* and *y.* If *x* '3 *y,* we have three possibilities: 0 - 0 = 0,
1 - 0 = 1, and 1 - 1 = O. The result is called the *difference bit.* If *x* < *y,* we have 0 - 1, and it is necessary to borrow a 1 from the next higher stage. The 1 borrowed from the next higher stage adds 2 to the minuend bit, just as in the decimal system a borrow adds 10 to a minuend digit. With the minuend equal to 2, the difference becomes
2 - 1 = 1. The half-subtractor needs two outputs. One output generates the difference and will be designated by the symbol *D.* The second output, designated *B* for borrow, generates the binary signal that informs the next stage that a 1 has been borrowed.
The truth table for the input-output relationships of a half-subtractor can now be derived as follows:

x	y	B	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

The Boolean functions for the two outputs of the half-subtractor are derived directly from the truth table:

$$D = x'y + xy' = x \oplus y$$

$$B = x'y$$

It is interesting to note that the logic for D is exactly the same as the logic for output S in the half-adder.

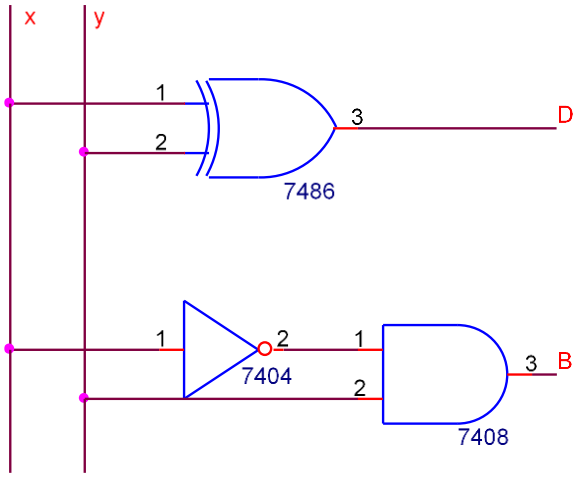


Fig 7.3. Half-subtractor

Full Subtractor

A full-subtractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. The three inputs, *x, y,* and z, denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, *D* and *B,* represent the difference and output borrow, respectively. The truth table for the circuit is

x	y	z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = x'y'z + x'yz' + xy'z' + xyz = x'(y'z + yz') + x(y'z' + yz) = x'(y \oplus z) + x(y \oplus z)' = x \oplus y \oplus z$$

$$B = x'y'z + x'yz' + x'yz + xyz = x'(y'z + yz') + yz(x' + x) = x'(y \oplus z) + yz$$

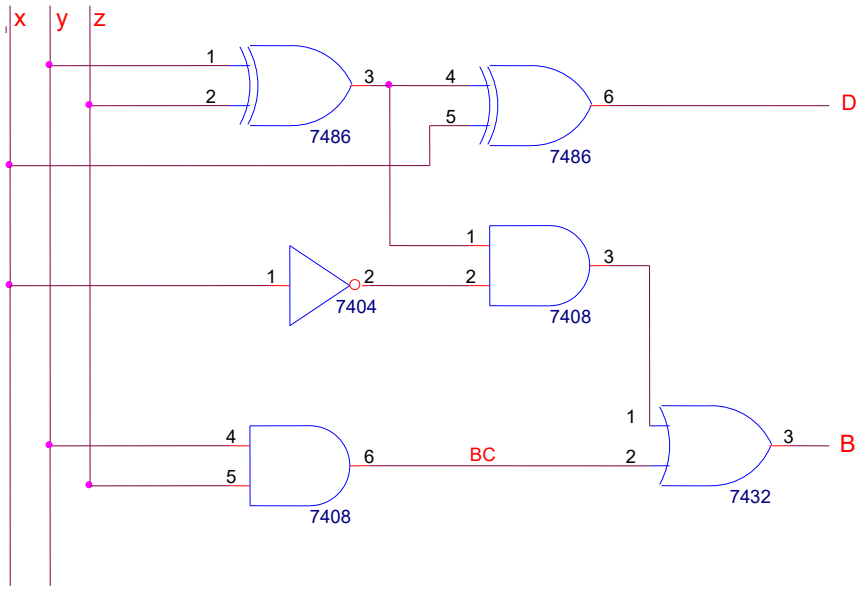


Fig 7.4. Full-subtractor

Caution:

1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate pins.

Equipment:

1. Trainer Board
2. IC 7400,7402,7404,7408,7432,7486
3. Microprocessor Data handbook

Procedure:

1. Fill up the truth table for a half adder
2. Verify the Boolean function for a half adder.
3. Construct the logic diagram from the Boolean functions.
4. Select the ICs from the equipment list.
5. Implement the output logic.
6. Repeat the whole procedure for half a subtractor.
7. Fill up the truth table for a full adder.
8. Verify the Boolean function for a full adder.
9. Construct the logic diagram from the Boolean functions.
10. Select the ICs from the equipment list.
11. Implement the output logic.
12. Repeat the whole procedure for a full sub tractor.

Report

1. Design a full adder using two half adder block and basic gates.

Experiment: 08
Experiment name: *Introduction to Multiplexers.*

Introduction
Multiplexers are the most important attributions of digital circuitry in communication hardware. These digital switches enable us to achieve the communication network we have today. In this experiment the students will have to construct MUX (as they call multiplexers) with simple logic gates and they will implement general logic using 8:1 MUX as the basic constructional unit.

Multiplexer
A modern home stereo system may have a switch that selects music from one of four sources: a cassette tape, a compact disc (CD), a radio tuner, or an auxiliary input such as audio from a VCR or DVD. The switch selects one of the electronic signals from one of these four sources and sends it to the power amplifier and speakers. In simple terms, this is what a **multiplexer (MUX)** does: it selects one of several input signals and passes it on to the output.

A digital multiplexer or data selector is a logic circuit that accepts several digital data inputs and selects one of them at any given time to pass on to the output. The routing of the desired data input to the output is controlled by SELECT inputs (often referred to as ADDRESS inputs). Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.
A 4 to l line multiplexer is shown in Figure. Each of the four input lines, I_0 to I_3 is applied to one input of an AND gate. Selection lines S_1 and S_0 are decoded to select a particular AND gate. The function table, Figure lists the input-to-output path for each possible bit combination of the selection lines. To demonstrate the circuit operation, consider the case when $S_1S_0 = 10$. The AND gate associated with input I_2 has two of its inputs equal to 1 and the third input connected to I_2. The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0. The OR gate output is now equal to the value of I_2 thus providing a path from the selected input to the output.

Caution:
1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate voltages to appropriate pins.

Equipment:
1. Trainer Board
2. IC 74151, 7432, 7408, 7404
3. Microprocessor Data handbook.

Job 1:
Implementation of a four to one way Multiplexer, (4:1 MUX) with basic gates.

Procedure:

1. Write the truth table for four to one way MUX.

S_1	S_0	Y

2. Write the Boolean function for the output logic.
3. Draw the logic diagram to implement the Boolean function.

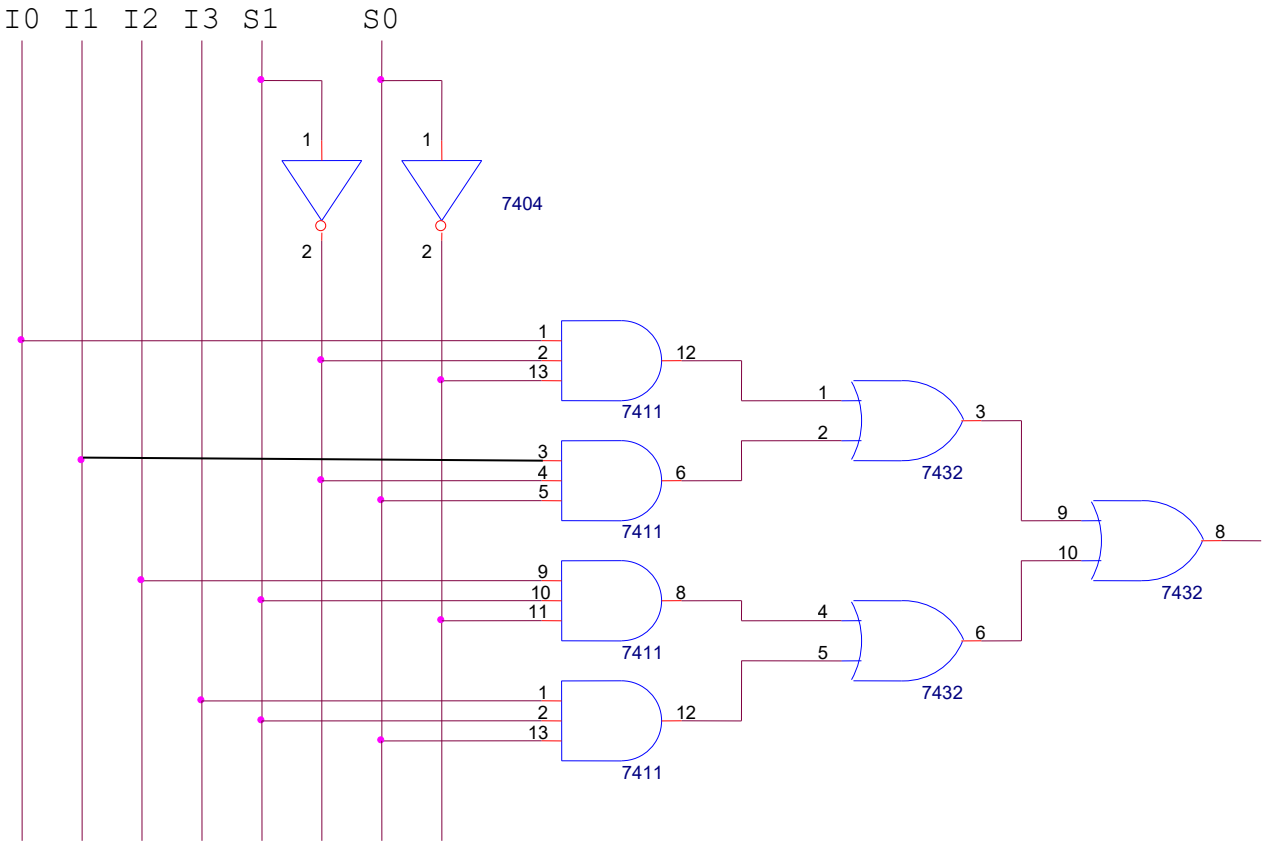


Figure 8.1: 4 to 1 Multiplexer

4. Select ICs from the equipment list.
5. Observe and note the output logic for all combination of inputs.

Job 2:

Implement the following function using an 8:1 MUX.

$$F(A,B,C,D)=\sum(0,1,3,5,8,9,14,15)$$

If we have a Boolean function of $n + 1$ variables, we take n of these variables and connect them to the selection lines of a multiplexer. The remaining single variable of the function is used for the inputs of the multiplexer. If A is this single variable, the inputs of the multiplexer are chosen

to be either A or A' or 1 or 0. By judicious use of these four values for the inputs and by connecting the other variables to the selection lines, one can implement any Boolean function with a multiplexer. In this way, it is possible to generate any function of $n + 1$ variables with a 2^n to1 multiplexer.

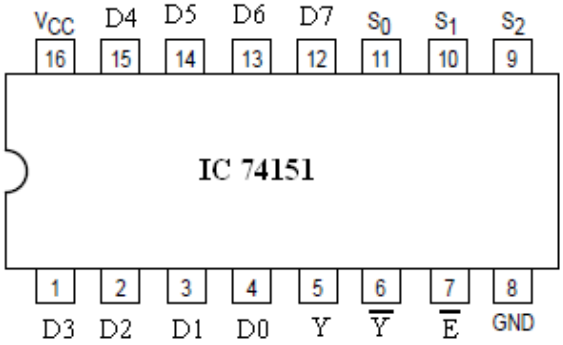


Fig 8.2. Pin diagram of IC 74151

Procedure:

1. Write the truth table for the above function.

A	*B*	*C*	*D*	*Y*
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Let, B, C, D of the 4 variables (A, B, C, D) are connected to the selection lines of a multiplexer and remaining single variable A of the function is used for the inputs of the multiplexer

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	1	1		1		1		
A	1	1					1	1
	1	**1**	**0**	A'	**0**	A'	A	A

2. Draw the logic diagram to implement the Boolean function.
3. Select ICs from the equipment list.
4. Observe and note the output logic for all combination of inputs.